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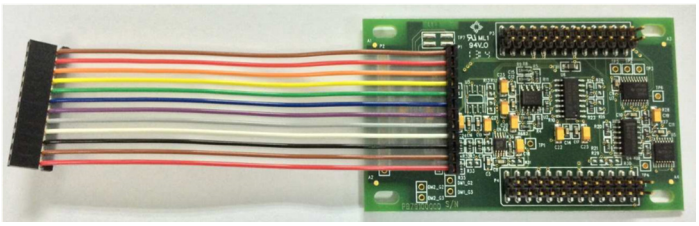
X-AIF

Analog Interface Board for X-Card/X-Card2 with X-DAQ

DATASHEET

DS0000080A



1. Features

X-AIF board is an analog interface board, which contains analog/digital buffers and drivers, together with the logical circuits to transfer the X-Card analog video signals to the video bus for further AD converting by the data acquisition board. Then the converted digital data is collected by the data acquisition and sent to the computer.

Amplifiers and analog switch on the X-AIF board are used to buffer and transfer the detector card video signal to the differential signal bus, and also transfer the digital control signals to the detector card. The X-AIF boards can be cascaded to connect to AD conversion channels.

Key Features:

- Can be cascaded by 26-pin flat cable.
- Interface for Low Energy and/or High Energy detector cards.
- Support of gain configuration capability for X-Card2 with 14-pin connection.

2. Ordering Information

DT Code	Part Name
13010972	X-AIF

3. General Description

X-AIF board can be used as analog interface board to connect the detector card (X-Card or X-Card2) with the data acquisition board (X-DAQ).

The typical schematic diagram is shown in Figure 1 with one AD chain of cascaded X-AIF boards. Up to 4 chains of X-AIF boards can be connected to one X-DAQ board. For details, please refer the X-DAQ datasheet.

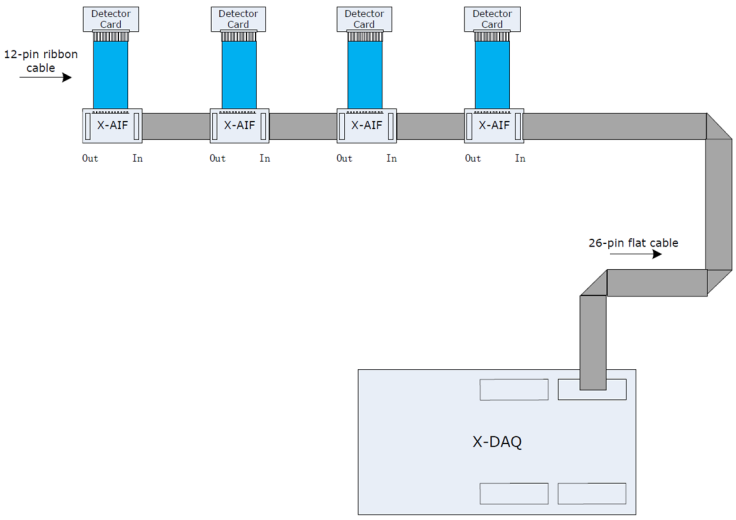


Figure 1. Block level diagram of detector read-out system

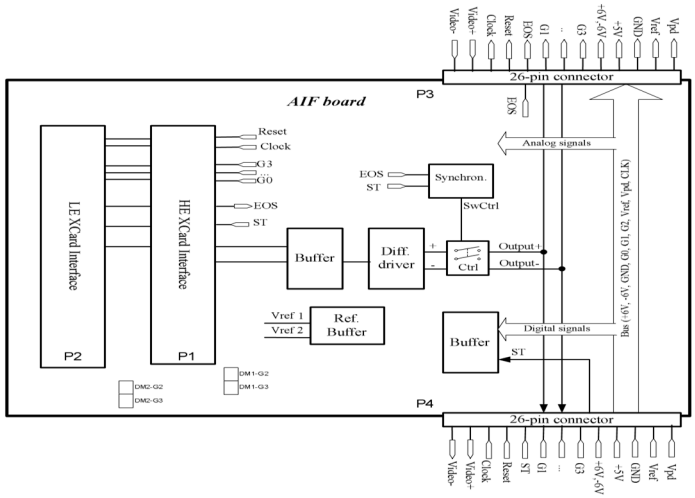


Figure 2. the block diagram of X-AIF board

The digital signals on the 26-pin signal bus are buffered and sent to the LE (Low Energy) and HE (High Energy) detector card interfaces as control timing, and the detector card sends out its video signal pixel by pixel. The amplifier then buffers the video signal to the amplifier of the differential driver, and the differential driver's output connects to the analog switch's input. The *"SwCtrl"* block generates the logic to control the analog switch output video signal or high-impedance to the signal bus, which allows the detector card video signals to be transferred to the common bus one by one in cascaded mode. The differential signal supports reliable transmission with long cable to the data acquisition board, so the data acquisition board can later convert the analog video signal to digital signals with digital signal processing.

4. X-AIF connection

The X-AIF board has following connections available.

- P1: 12-pin IDC cable and connector for the detector card. By default, the 12-pin IDC cable is soldered on the X-AIF board. Both X-Card and X-Card2 products can be supported as detector cards, which are shown below in Table 1.

Table 1. the detector cards supported by X-AIF board

DT Code	Part Name
13010153	X-Card 0.2-256NG
13010148	X-Card 0.4-128G
13010152	X-Card 0.4-128NG
13010146	X-Card 0.8-64G
13010151	X-Card 0.8-64NG
13010150	X-Card 0.8-128G
13010458	X-Card2 0.2-256G
13010457	X-Card2 0.4-128G
13010456	X-Card2 0.8-64G
13012132	X-Card2 0.2-256CWO
13012133	X-Card2 0.4-128CWO

- P2: Reserved 12-pin connector for dual energy configuration.
- P3: 26-pin ribbon cable connector header for signal bus cable (Input).
- P4: 26-pin ribbon cable connector header for signal bus cable (Output). The last one of the daisy chain should connect the data acquisition board. Supported data acquisition boards are listed in the table below.

DT Code	Part Name
13011510	X-DAQ ENET-UDP
13010071	X-DAQ USB

4.1. Interface with the detector card

P1: 12-pin connector. The pin definition is listed in

Table 2.

- Type: IDMS-12-T-2-R
- Mating with: TSW-112-08-G-S-RA
- Supplier: Samtec

Table 2. External pin definition of 12-pin connector (P1) of X-AIF board

Pin Number	Symbol	Description	Note
1	RST	Reset signal	Digital pulse input
2	CLK	Main clock	Digital pulse input
3	TRIGGER	Trigger signal	Digital pulse input
4	START	Start signal	Digital pulse input
5	M/S	Master/Slave signal	Digital pulse input
6	+5V	+5V Power supply	Power Supply input
7	GND	Ground	Voltage input
8	EOS	EOS signal	Digital output
9	Video	X-Card Video signal	Analog voltage output
10	Vref	Reference voltage	Voltage input
11	G1	Gain selection pin	Digital level input
12	Vpd	Vpd power supply	Power Supply input

4.2. 26-pin IDC pin header (P3 and P4)

P3 and P4: 2.54mm dual rows pin headers. The pin definition of 26-pin IDC header (P3 and P4) is listed in Table 3 below.

Table 3. The pin definition of 26-pin IDC header (P3 and P4) of X-AIF board

Pin Number	Symbol	Description	Note
1, 2, 5, 6, 11, 12, 18, 20, 22, 24	GND	Ground	Voltage input
15, 16	+5V	+5V power supply	Voltage input
7, 8	+6V	+6V power supply	Voltage input
9, 10	-6V	-6V power supply	Voltage input
13	Video+	Positive node of differential output	Analog voltage output
14	Video-	Negative node of differential output	Analog voltage output
3	Vref	Reference voltage	Voltage input
4	Vpd	Power supply	Voltage input
17	EOS	EOS signal	Digital output
19	CLK	Main clock	Digital pulse input
21	RESET	Reset pulse	Digital pulse input
23	G1	Gain selection pin 1 (lowest)	Digital level input
25	G2	Gain selection pin 2	Digital level input
26	G3	Gain selection pin 3	Digital level input

5. Gain selection

By default, only two gains (0.5pf and 1pf) are enabled, as 12-pin IDC cable and connector is used in P1. In order to enable 8 gains configuration with X-Card2 products, two jumping wires on DM1-G2 and DM2-G3 of XAIF board can be connected to extra two pin holes of X-Card2.

The picture 3 below is an example of how to enable 8 gains options with X-Card2 by two jumping wires.

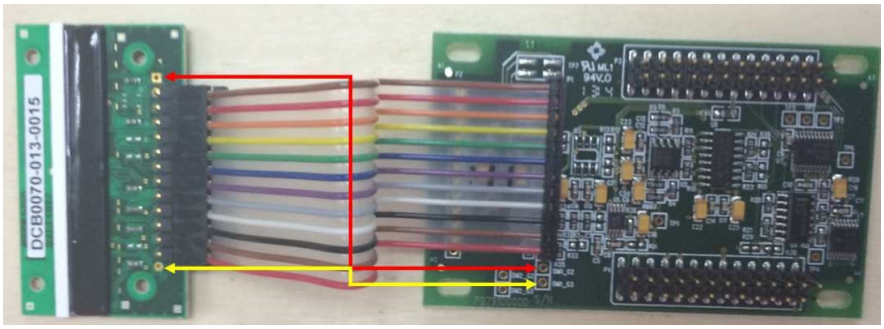


Figure 3. How to enable the 8 gain options with X-Card2 by 2 jumping wires

6. Electrical Characteristics

Absolute maximum electrical ratings are listed in Table 4, the recommended operating conditions are listed in Table 5, and the typical power dissipation is listed in Table 6.

Table 4. Maximum electrical ratings

Parameter	Symbol	Unit	Min.	Max.
Power supply voltage	+5VD	V	-0.3	+ 6.0
Power supply voltage	Vref, VPD	V	-0.3	+ 6.0
Power supply voltage	+6V	V	-0.3	+12
Power supply voltage	-6V	V	-12	+0.3
Clock pulse voltage	CLK	V	-0.3	+ 6.0
Reset pulse voltage	Reset	V	-0.3	+ 6.0
Gain selection	G1, G2, G3	V	-0.3	+ 6.0
Operating temperature	T_{opt}	°C	0	+50
Storage temperature	T_{stg}	°C	-10	+60
Operating humidity at 30°C	Rhd	%		85
Storage humidity at 40 °C	Rhd	%		95

Table 5. Recommended Operating Conditions

Parameter		Symbol	Unit	Min.	Typ.	Max.
Power supply voltage		+5VD	V	4.75	5	5.25
Power supply voltage		+6V	V	5.75	6	6.25
Power supply voltage		-6V	V	-6.25	-6	-5.75
Reference voltage		Vref, Vpd	V	3.5	4	Vcc
Clock pulse voltage	High level	Clk	V	Vcc -0.25	Vcc	Vcc +0.25
	Low level		V	0	-	0.4
Gain selection	High level	G1, G2, G3	V	Vcc -0.25	Vcc	Vcc +0.25
	Low level		V	0	-	0.4
Reset pulse voltage	High level	RESET	V	Vcc -0.25	Vcc	Vcc +0.25
	Low level		V	0	-	0.4

Table 6. Typical Power Dissipation

Power supply	Symbol	Unit	Typ.
Power supply voltage	V_{cc} (+5V)	mA	23
Power supply voltage	+,- 6V	mA	24

7. Timing Diagram

The X-AIF board needs to be be used together with the detector card, and the timing diagram provided here is for the X-AIF board and the detector card together. The internal timing is triggered by the falling edge of the Reset signal. The integrated signal from previous integration period is first sampled and hold (S/H) during period of 8 clock cycles. The feedback capacitance of the charge amplifier is then reset. The integration period starts 8 clock cycles after the rising edge of Reset signal and stops at 8 clock cycles after the next falling edge of Reset.

The video signal readout is controlled by START signal, and the video signal output is always delayed by one integration cycle, which means, at integration cycle N, the module outputs the results from cycle N-1.Figure 3 shows the timing principles, and Figure 4 shows the signal timing specifications in greater details.

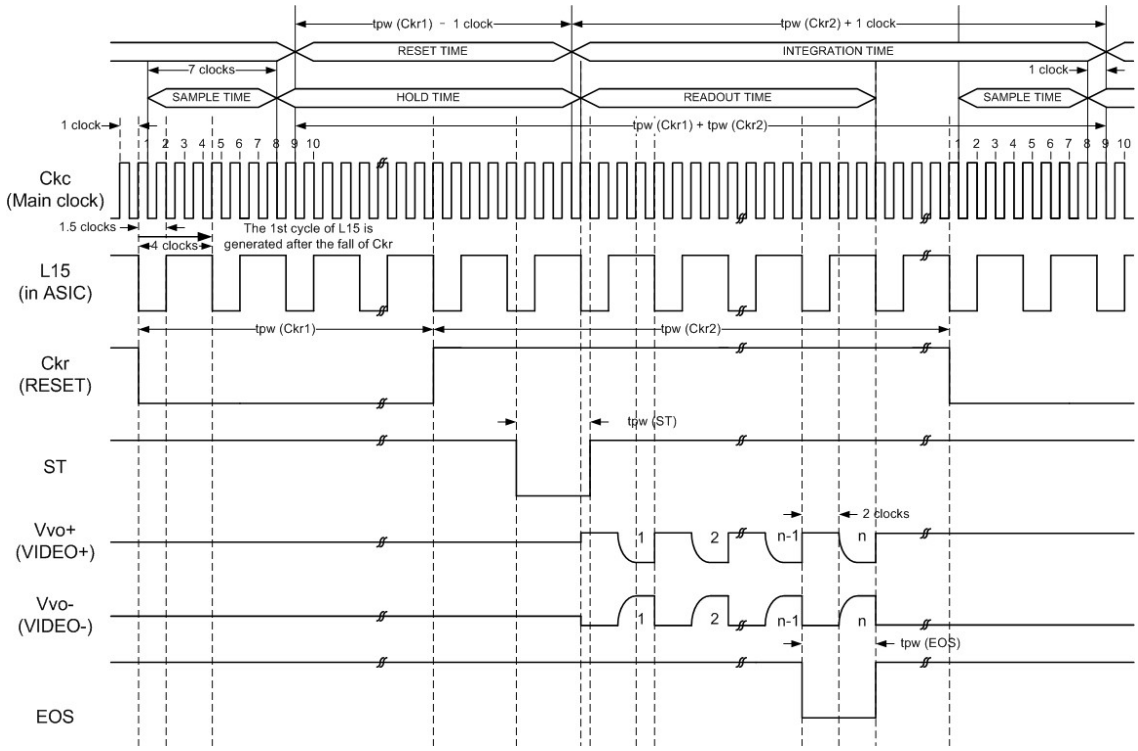


Figure 4. External timing diagram of the X-AIF with the detector card

Notes:

1. Ckr is set on the RISING edge of Ckc.
2. Ckr is sampled on the FALLING edge of Ckc.
3. ST is set on the FALLING edge of Ckc.
4. ST is sampled on the RISING edge of Ckc.
5. ST is only denoted as the first EOS signal generated from system.
6. The first channel output of Vvo should be generated outside the RISING edge of Ckr.
7. The first channel output of Vvo is generated on the FALLING edge of L15 (in ASIC).
8. EOS is generated on the RISING edge of Ckc.

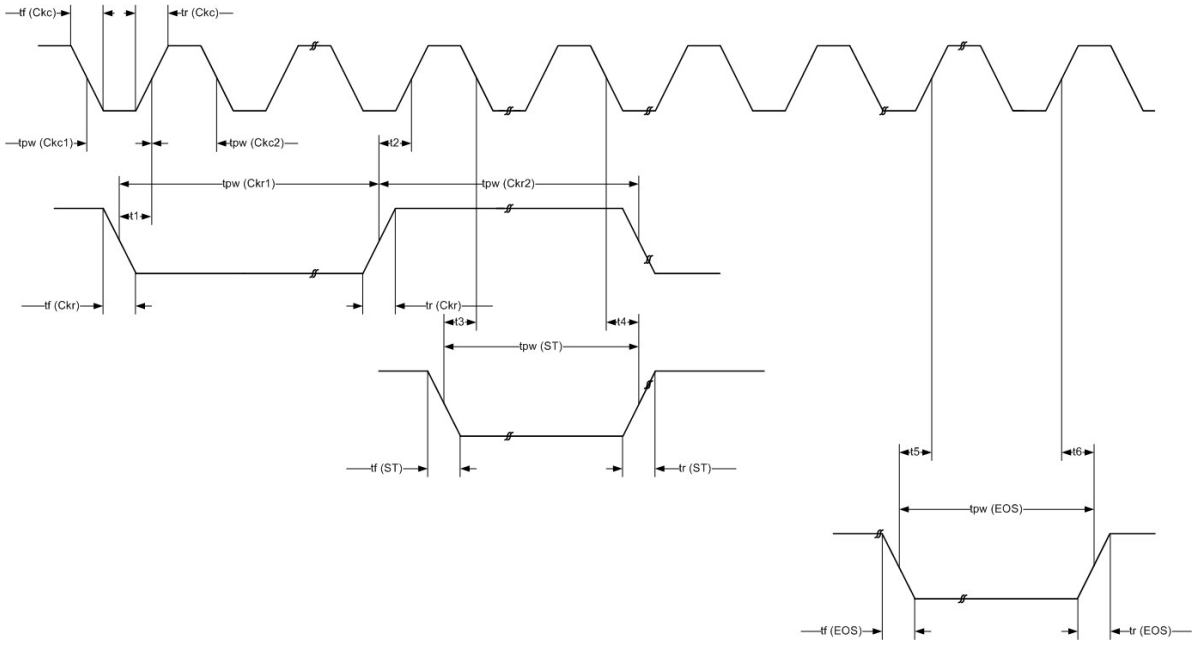


Figure 5. The detailed timing diagram of the X-AIF with the detector card

Table 7. Timing parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Ckc pulse width	tpw (Ckc1), tpw (Ckc2)	125	-	12500	ns
Ckc pulse rise/fall times	tr (Ckc), tf (Ckc)	0	20	30	ns
Ckr pulse width 1	tpw (Ckr1)	*	-	-	us
Ckr pulse width 2	tpw (Ckr2)	130	-	-	us
Ckr pulse rise/fall times	tr (Ckr), tf (Ckr)	0	20	30	ns
Ckc pulse-Ckr pulse timing 1	t1	-20	0	20	ns
Ckc pulse-Ckr pulse timing 2	t2	-20	0	20	ns
ST pulse width	tpw (ST)	4 clocks			-
ST pulse rise/fall times	tr (ST), tf (ST)	0	20	30	ns
Ckc pulse-ST pulse timing 3	t3	-20	0	20	ns
Ckc pulse-ST pulse timing 4	t4	-20	0	20	ns
EOS pulse width	tpw (EOS)	4 clocks			-
EOS pulse rise/fall times	tr (EOS), tf (EOS)	0	20	30	ns
Ckc pulse-EOS pulse timing 5	t5	-20	0	20	ns
Ckc pulse-EOS pulse timing 6	t6	-20	0	20	ns

* The min value of tpw (Ckr1) in X-Card is 10us, and 30us in 0.4mm X-Card2, and 20us in 0.8mm X-Card2 and 0.2mm X-Card2.

8. Cascading

The X-AIF boards can be cascaded together in each AD conversion channel. The configuration is shown in Figure 6. The Reset pulse is sent to all the X-AIF boards in the daisy chain at the same time, and the integration cycle is done simultaneously. A START (ST) signal, as shown in Figure 7 in previous section, is sent to the first X-AIF board to trigger the readout. After all pixels in the 1st X-AIF and the connected detector card have been read out, EOS signal is sent from the first X-AIF board to the second X-AIF board as the ST signal. The readout of the 2nd X-AIF board is then triggered. Because all X-AIF boards share the same signal bus, on the video bus, the signals from each X-AIF board are read out pixel by pixel continuously to X-DAQ board. Please refer to X-DAQ datasheet for more information.

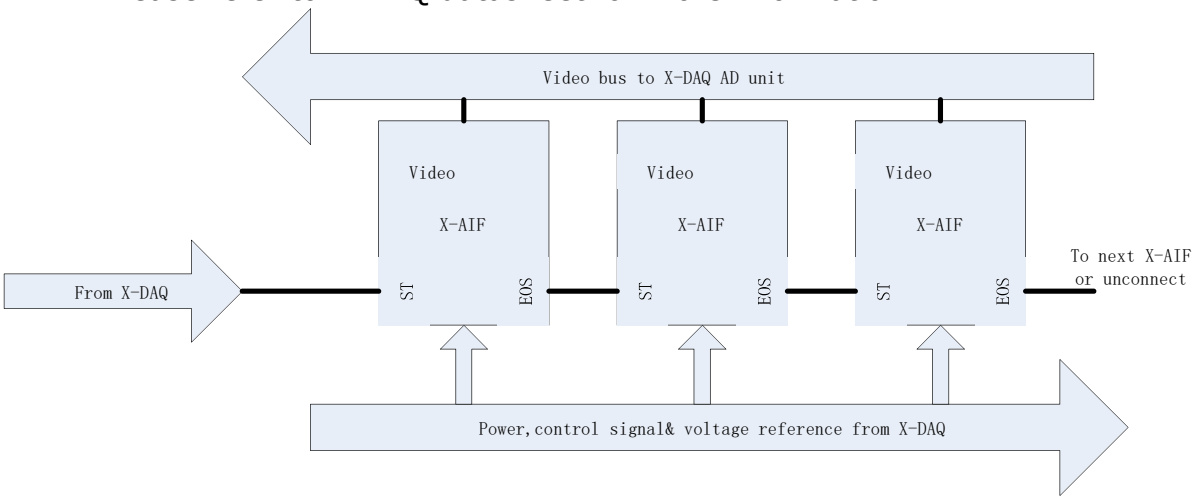


Figure 6. The X-AIF cascading configuration

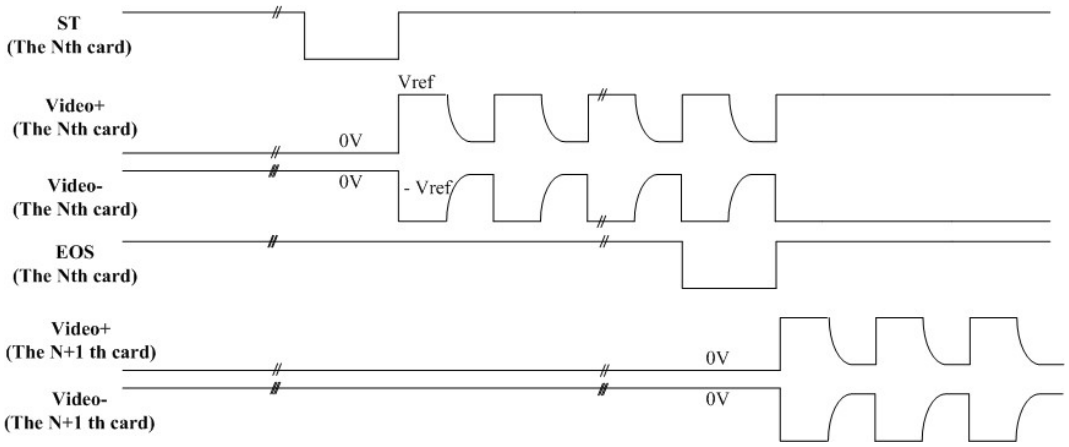


Figure 7. Readout timing of cascaded X-AIF and the detector card package

9. Mechanical Dimensions

The X-AIF board mechanical dimensions and mounting holes are shown in Figure 8 below.

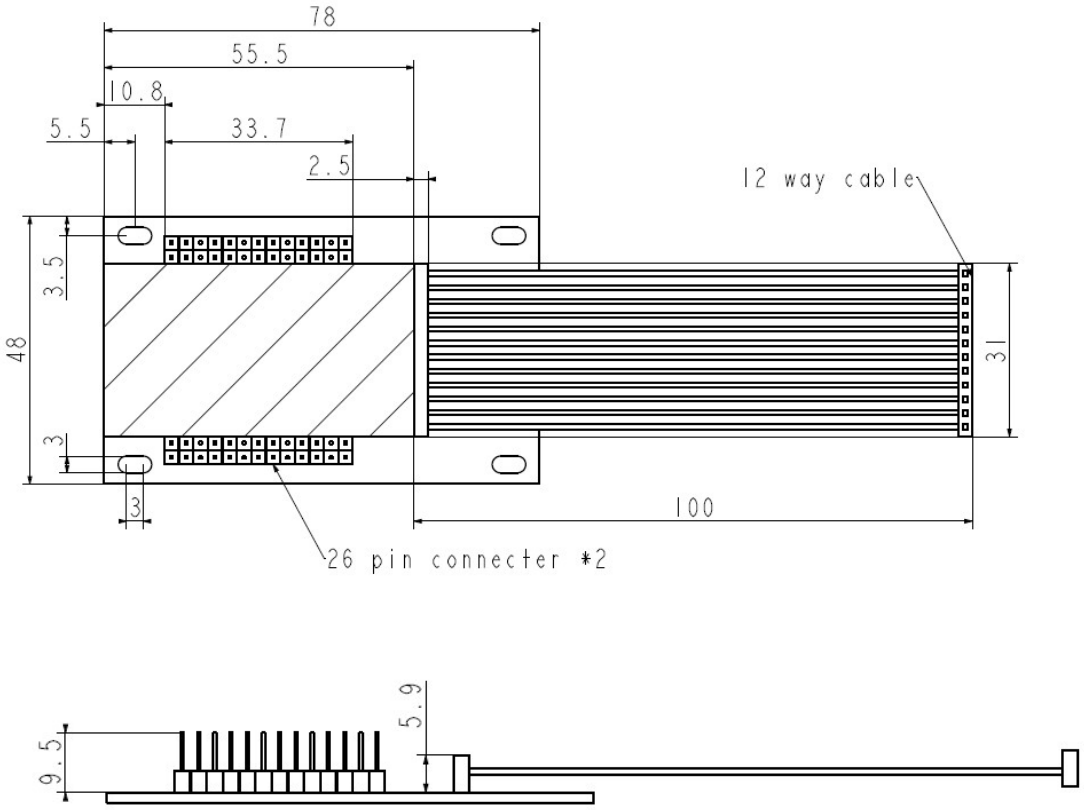


Figure 8. X-AIF board mechanical dimension

Change Record

Revision	Date issued	Person	Description of Change
Draft	2014.01.23	Li Bidan	Draft version
A	2014.01.29	Wang Fei	Initial release version
B	2015.09.01	M Sammons	Detector readout diagram updated